The listing of claims will replace all prior versions, and listings, of claims in the application:

Listing of Claims:

1. (Currently Amended) An electric device comprising:

an insulating substrate;

an active matrix circuit including at least one thin film transistor formed over a first surface of said insulating substrate;

a driving circuit including at least another one thin film transistor for driving the active matrix circuit formed over said first surface of the insulating substrate;

a counter substrate facing the first surface of said insulating substrate with a gap therebetween, said counter substrate covering said active matrix circuit and said driving circuit wherein said insulating substrate extends beyond at least one side edge of the counter substrate so as to provide an extended portion; and

at least one semiconductor integrated circuit chip disposed over said first surface of the extended portion of the insulating substrate and operationally connected with the driving circuit wherein said integrated circuit chip is ~~at least one of a memory, an input port, a correction memory and a CPU~~ electrically connected to a wiring comprising indium tin oxide formed over said insulating substrate,

wherein said at least one thin film transistor and said at least another one thin film transistor are formed from a common semiconductor film formed over the first surface of the insulating substrate.

2. (Previously Presented) The device of claim 1 wherein the semiconductor integrated circuit chip is connected with the driving circuit by a wire bonding.

3. (Previously Presented) The device of claim 1 wherein the semiconductor integrated circuit chip is connected with the driving circuit by a COG (chip on glass).

4. - 5. (Canceled)

6. (Previously Presented) The device of claim 1 wherein the insulating substrate comprises a glass substrate.

7. (Currently Amended) A display device comprising:

a first substrate having a first surface;

an active matrix circuit including at least one thin film transistor formed over the first substrate;

a driving circuit including at least another one thin film transistor for driving the active matrix circuit formed over the first substrate;

a second substrate facing said first substrate with a gap therebetween, said first substrate having an extended portion which extends beyond at least one side edge of the second substrate; and

at least one semiconductor integrated circuit chip disposed over the first substrate and operationally connected to said driving circuit wherein said semiconductor integrated circuit chip is ~~at least one of a memory, an input port, and a CPU~~ electrically connected to a wiring comprising indium tin oxide formed over said first substrate,

wherein said at least one thin film transistor and said at least another one thin film transistor are formed from a common semiconductor film formed over the first substrate, and

wherein said at least one thin film transistor of the active matrix circuit has at least one lightly doped drain between a channel region and a drain region thereof.

8. (Canceled)

9. (Previously Presented) The device of claim 7 wherein said memory is a correction memory.

10. (Previously Presented) The device of claim 7 further comprising a liquid crystal adjacent to said active matrix circuit.

11. - 16. (Canceled)

17. (Currently Amended) An electric device comprising:

a first substrate having an insulating surface;

a plurality of thin film transistors formed on the insulating surface, said plurality of thin film transistors being formed from a common semiconductor film formed on said insulating surface;

a second substrate facing said first substrate with a gap therebetween, said first substrate having an extended portion which extends beyond at least one side edge of the second substrate; and

at least one single crystalline semiconductor integrated circuit chip formed on the insulating surface wherein said semiconductor integrated circuit chip is ~~at least one of a memory, an input port, a correction memory and a CPU~~ electrically connected to a wiring comprising indium tin oxide formed over said first substrate,

wherein at least one of the thin film transistors is provided as an active matrix circuit, at least another one of the thin film transistors is provided as at least one driving circuit for driving the active matrix circuit and the semiconductor integrated circuit chip is provided as a control circuit for controlling the driving circuit, and wherein said common semiconductor film is formed by crystallizing a semiconductor film comprising amorphous silicon deposited on said insulating surface.

18. (Previously Presented) The device of claim 17 wherein the first substrate comprises a glass substrate.

19. (Original) The device of claim 17 wherein the semiconductor integrated circuit chip is connected with the driving circuit by a wire bonding.

20. (Previously Presented) The device of claim 17 wherein the semiconductor integrated circuit chip is connected with the driving circuit by a COG (chip on glass).

21. (Currently Amended) An electric device comprising:

a first substrate;

an active matrix circuit formed over said first substrate with at least one thin film transistor;

a driving circuit formed over said first substrate with at least one other thin film transistor for driving the active matrix circuit;

a second substrate facing said first substrate with a gap therebetween, said first substrate extending beyond at least one side edge of the second substrate to provide an extended portion wherein said second substrate covers said active matrix circuit and said driving circuit; and

a semiconductor integrated circuit chip disposed over the extended portion of said first substrate and operationally connected to said driving circuit wherein said integrated circuit chip is ~~at least one of a memory, an input port, a correction memory and a CPU~~ electrically connected to a wiring comprising indium tin oxide formed over said first substrate,

wherein said at least one thin film transistor and said one other thin film transistor are formed from a common semiconductor film obtained by crystallizing a semiconductor film comprising amorphous silicon deposited over said first substrate.

22. (Original) The device of claim 21 wherein the other thin film transistor is a complementary type.

23. (Original) The device of claim 21 wherein the other thin film transistor has only P-type TFT.

24. (Original) The device of claim 21 wherein the other thin film transistor has only N-type TFT.

25. (Canceled)

26. (Previously Presented) The device of claim 1 wherein the thin film transistor of the active matrix circuit has the same structure as that of the thin film transistor of the driver circuit.

27. (Previously Presented) The device of claim 7 wherein the thin film transistor of the active matrix circuit has the same structure as that of the thin film transistor of the driver circuit.

28. - 29. (Canceled)

30. (Previously Presented) The device of claim 17 wherein the thin film transistor of the active matrix circuit has the same structure as that of the thin film transistor of the driver circuit.

31. (Previously Presented) The device of claim 21 wherein the thin film transistor of the active matrix circuit has the same structure as that of the thin film transistor of the driver circuit.

32. (Currently Amended) A display device comprising:

a first substrate having an insulating surface;

an active matrix circuit including a first plurality of thin film transistors formed on the insulating surface of the first substrate;

a driving circuit including a second plurality of thin film transistors formed over the insulating surface of the first substrate for driving said active matrix circuit;

a second substrate facing said first substrate with a liquid crystal material interposed therebetween, said first substrate having an extended portion which extends beyond at least one side edge of the second substrate wherein said second substrate covers said active matrix circuit and said driving circuit; and

at least one semiconductor integrated circuit chip disposed over the extended portion of the first substrate and operationally connected to said driving circuit wherein said integrated circuit chip is ~~at least one of a memory, an input port, a correction memory and a CPU~~ electrically connected to a wiring comprising indium tin oxide formed over said first substrate,

wherein said first and second plurality of thin film transistors are formed from a common semiconductor film formed over said first substrate, and each of said first plurality of thin film transistors has at least one lightly doped drain between a channel region and a drain region thereof.

33. (Previously Presented) A display device according to claim 32 wherein said semiconductor film comprises crystalline silicon.

34. - 35. (Canceled)

36. (Currently Amended) A display device comprising:

a first substrate having an insulating surface;

an active matrix circuit including a first plurality of thin film transistors formed on the insulating surface of the first substrate;

a driving circuit including a second plurality of thin film transistors formed over the insulating surface of the first substrate for driving said active matrix circuit;

a second substrate facing said first substrate with a gap therebetween, said first substrate having an extended portion which extends beyond at least one side edge of the second substrate wherein said second substrate covers said active matrix circuit and said driving circuit; and

at least one semiconductor integrated circuit chip disposed over the extended portion of the first substrate and ~~operationally connected to said driving circuit~~ electrically connected to a wiring comprising indium tin oxide formed over said first substrate,

wherein each of said first plurality of thin film transistors is a bottom gate type transistor in which a gate electrode is located below a channel region of the transistor, and each of said second plurality of thin film transistors is a top gate type transistor in which a gate electrode is located over a channel region of the transistor.

37. (Previously Presented) A device according to claim 36 wherein the channel region of each of the first plurality of thin film transistors is amorphous while the channel region of each of the second plurality of thin film transistors is crystalline.

38. (Currently Amended) A display device comprising:

a first substrate having an insulating surface;

an active matrix circuit including a first plurality of thin film transistors formed on the insulating surface of the first substrate;

a driving circuit including a second plurality of thin film transistors formed over the insulating surface of the first substrate for driving said active matrix circuit; and

a second substrate facing said first substrate with a gap therebetween, said first substrate having an extended portion which extends beyond at least one side edge of the second substrate;

at least one semiconductor integrated circuit chip disposed over the extended portion of the first substrate and operationally connected to said driving circuit,

wherein said semiconductor integrated circuit chip is ~~selected from the group consisting of a correction memory, a memory, a CPU, and an input port~~ electrically connected to a wiring comprising indium tin oxide formed over said first substrate.

39. (Previously Presented) A device according to claim 38 wherein the channel region of each of the first plurality of thin film transistors is amorphous while the channel region of each of the second plurality of thin film transistors is crystalline.

40. (Previously Presented) The device according to claim 1 further comprising a liquid crystal material disposed between said insulating substrate and said counter substrate.

41. (Previously Presented) The device according to claim 21 further comprising a liquid crystal material disposed between said first and second substrates.

42. (Previously Presented) The device according to claim 36 further comprising a liquid crystal material disposed between said first and second substrates.

43. (Previously Presented) The device according to claim 38 further comprising a liquid crystal material disposed between said first and second substrates.

44. - 50. (Canceled)

51. (Currently Amended) An electric device comprising:

a first insulating substrate;

an active matrix circuit including at least one thin film transistor formed over said first insulating substrate;

a driving circuit including at least another one thin film transistor for driving the active matrix circuit formed over said first insulating substrate;

a second substrate facing said first insulating substrate with a gap therebetween, said first insulating substrate having an extended portion which extends beyond at least one side edge of the second substrate; and

at least one semiconductor integrated circuit chip disposed over said first insulating substrate and operationally connected with the driving circuit wherein said integrated circuit chip is ~~at least one of a memory, an input port, a correction memory and a CPU~~ electrically connected to a wiring comprising indium tin oxide formed over said first substrate,

wherein said at least one thin film transistor and said at least another one thin film transistor are formed from a common semiconductor film formed over the first insulating substrate, and

wherein said at least one thin film transistor of the active matrix circuit has at least one lightly doped drain between a channel region and a drain region thereof.

52. (Previously Presented) The device of claim 51 wherein the semiconductor integrated circuit chip is connected with the driving circuit by a wire bonding.

53. (Previously Presented) The device of claim 51 wherein the semiconductor integrated circuit chip is connected with the driving circuit by a COG (chip on glass).

54. (Previously Presented) The device of claim 51 wherein the first insulating substrate comprises a glass substrate.

55. (Canceled)

56. (New) The device according to claim 1 wherein said semiconductor integrated circuit chip is at least one selected from the group consisting of a memory, an input port, a correction memory, and a CPU.

57. (New) The device according to claim 7 wherein said semiconductor integrated circuit chip is at least one selected from the group consisting of a memory, an input port, and a CPU.

58. (New) The device according to claim 17 wherein said semiconductor integrated circuit chip is at least one selected from the group consisting of a memory, an input port, a correction memory, and a CPU.

59. (New) The device according to claim 21 wherein said semiconductor integrated circuit chip is at least one selected from the group consisting of a memory, an input port, a correction memory, and a CPU.

60. (New) The device according to claim 32 wherein said semiconductor integrated circuit chip is at least one selected from the group consisting of a memory, an input port, a correction memory, and a CPU.

61. (New) The device according to claim 36 wherein said semiconductor integrated circuit chip is at least one selected from the group consisting of a memory, an input port, a correction memory, and a CPU.

62. (New) The device according to claim 38 wherein said semiconductor integrated circuit chip is at least one selected from the group consisting of a memory, an input port, a correction memory, and a CPU.

63. (New) The device according to claim 51 wherein said semiconductor integrated circuit chip is at least one selected from the group consisting of a memory, an input port, a correction memory, and a CPU.